EQD200-SR8

200G QSFP-DD SR8 Optical Transceiver

PRODUCT FEATURES

- Supports 206.2 Gbps Aggregate Bit Rates
- Single 3.3V Power Supply and Power Dissipation < 5W
- Up to 70m Transmission on MMF OM3, and 100m Transmission on MMF OM4
- MPO-12 Two Row Connector PC
- Safety Certification: TUV/UL/FDA*1
- Operating Case Temperature: 0°C~+70°C
- Compliant with QSFP-DD MSA Specification
- I2C interface with integrated Digital Diagnostic Monitoring
- RoHS compliant (lead-free) *1

APPLICATIONS

- 200G SR8 applications
- 2x100G application

DESCRIPTIONS

The EQD200-SR8 8x25G transceiver module is designed for use in 200 Gigabit Ethernet links up to 100m over OM4 and 70m over OM3 multi-mode fiber. The module has 8 independent electrical input/output channels operating at 25.78125Gbp/s per channel. This transceiver consists of two transmitter/receiver units, with each operating on 850nm wavelength. The transmitter path of the module incorporates CDR with two 4-channel modulator drivers and 8 modulated lasers. On the receiver path, it consists of 8 photodiodes and two 4-channel TIAs, along with the CDR. The electrical interface of the module is compliant with the CAUI-4 interface as defined by IEEE 802.3bm, and compliant with QSFP-DD MSA.

Module Block Diagram

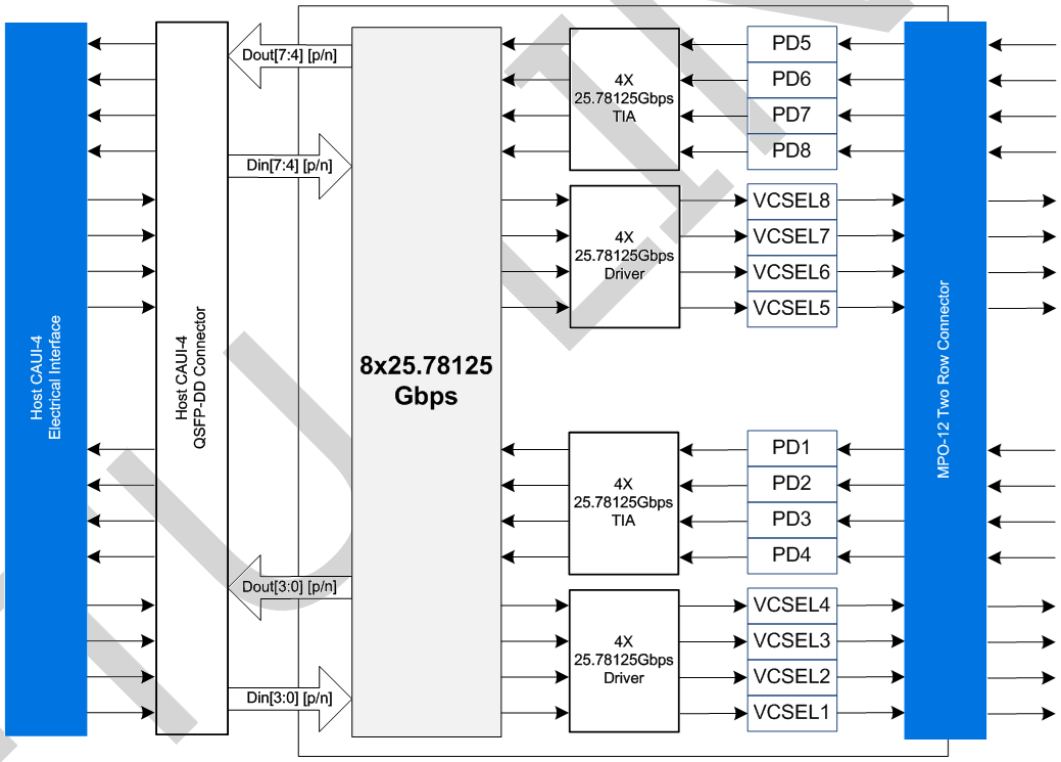


Figure 1: Transceiver Block Diagram

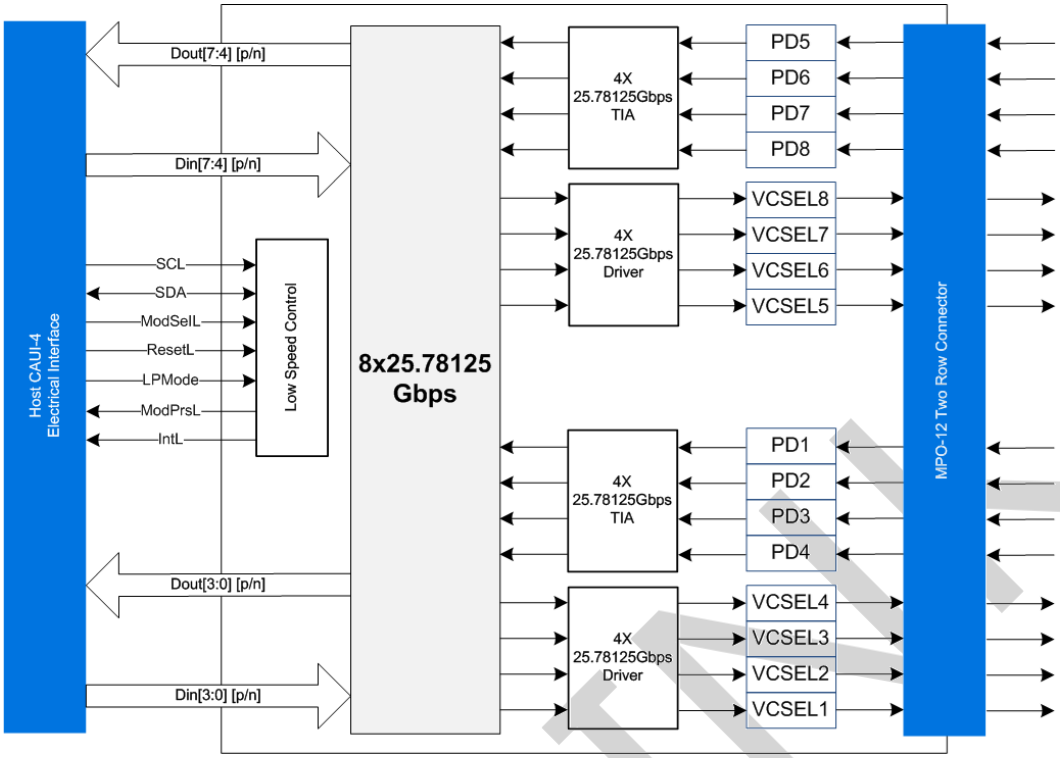


Figure 2: Application Reference Diagram

Ordering Information

Part No.	Data Rate(optical)	Laser	Fiber Type	Distance	Optical Interface	Temp	DDMI	CMIS
EQD200-SR8	206.2Gbps	VCSEL	OM4/ OM3	100m/ 70m	MPO-12 Two Row PC	0~70□	Yes	CMIS4.0*3

Notes:

1. For the latest certification information, please check with ETU.
2. Over MMF.
3. CMIS4.0 or later version.

Transmitter

As shown in Figure 1, the transmitter part of the transceiver contains an 8x25.78125Gbps CAUI-4 electrical input and equalization (EQ) block, two 4-channel laser drivers and a multi-mode laser source.

Receiver

As shown in Figure 1, the receiver part of the transceiver contains eight PIN photodiodes, two 4-channel trans-

impedance amplifiers (TIA), and an integrated 8x25.78125Gbps CAUI-4 compatible electrical output module.

High Speed Electrical Signal Interface

The interface between QSFP-DD module and ASIC/SerDes is shown in Figure 2. The high speed signal lines are internally AC-coupled and the electrical inputs are internally terminated to 100 ohms' differential. All transmitter and receiver electrical channels are compliant to C2M CAUI-4 specifications per IEEE 802.3bm.

Control Signal Interface

The following pin is provided to control module or display the module status: ModSelL, ResetL, ModPrsL, IntL and LPMode. In addition, there is an industry standard two wire serial interface scaled for 3.3V LVTTL. The definition of control signal interface and the registers of the serial interface memory are defined in the Control Interface & Memory Map section.

Handling and Cleaning

Exposure to current surges and overvoltage events can cause immediate damage to the transceiver module. Observe the precautions for normal operation of electrostatic discharge sensitive equipment; Attention shall also be paid to limiting transceiver module exposure to conditions beyond those specified in the absolute maximum ratings.

Optical connectors include female connectors. These elements will be exposed as long as the cable or port plug is not inserted. At this time, always pay attention to protection.

Each module is equipped with a port guard plug to protect the optical port. The protective plug shall always be in place whenever the optical fiber is not inserted. Before inserting the optical fiber, it is recommended to clean the end of the optical fiber connector to avoid contamination of the module optical port due to dirty connector. If contamination occurs, use standard MPO port cleaning methods.

Absolute Maximum Ratings

Exceeding the absolute maximum ratings table may cause permanent damage to the device. This is just an emphasized rating, and does not involve the functional operation of the device that exceeds the specifications of this technical specification under these or other conditions. Long-term operation under absolute maximum ratings will affect the reliability of the device.

Parameter	Symbol	Min.	Typical	Max.	Unit
Storage Temperature	Ts	-40		85	□
3.3 V Power Supply Voltage	Vcc	-0.5	3.3	3.6	V

Relative Humidity	RH	5		85	%

Recommended Operating Conditions

For operations beyond the recommended operating conditions, optical and electrical characteristics are not defined, reliability is not implied, and such operations for a long time may damage the module.

Parameter	Symbol	Min.	Typical	Max.	Unit
Operating Case Temperature	Tc	0		70	°C
Power Supply Voltage	Vcc	3.135	3.3	3.465	V
Power Supply Noise *5				25	mVpp
Receiver Differential Data Output Load			100		Ohm
Fiber Length (MMF)	OM3			70	m
	OM4			100	m

Notes:

1. Power Supply specifications, Instantaneous, sustained and steady state current compliant with QSFP-DD MSA Power Classification.
2. Power Supply Noise is defined as the peak-to-peak noise amplitude over the frequency range at the host supply side of the recommended power supply filter with the module and recommended filter in place. Voltage levels including peak-to-peak noise are limited to the recommended operating range of the associated power supply. See Figure 9 for recommended power supply filter.

Electrical Characteristics

Unless otherwise stated, the following characteristics are defined under recommended operating conditions.

Parameter	Symbol	Min.	Typical	Max.	Unit
Transceiver Power Consumption				5	W
Transceiver Power Supply Total Current				1515	mA
AC Coupling Internal Capacitor			0.1		μF

Note:

1. For control signal timing including ModSelL, ResetL, IntL, LPMode, SCL and SDA see Control Interface Section.

Reference Points

Test Point	Description
TP1 and TP4	TP1 and TP4 are informative reference points that may be useful to implementers for testing components.
TP2	Unless specified otherwise, all transmitter measurements defined in 802.3bm 95.7.1 are made at TP2.

TP3	Unless specified otherwise, all receiver measurements and tests defined in 802.3bm 95.7.2 are made at TP3.

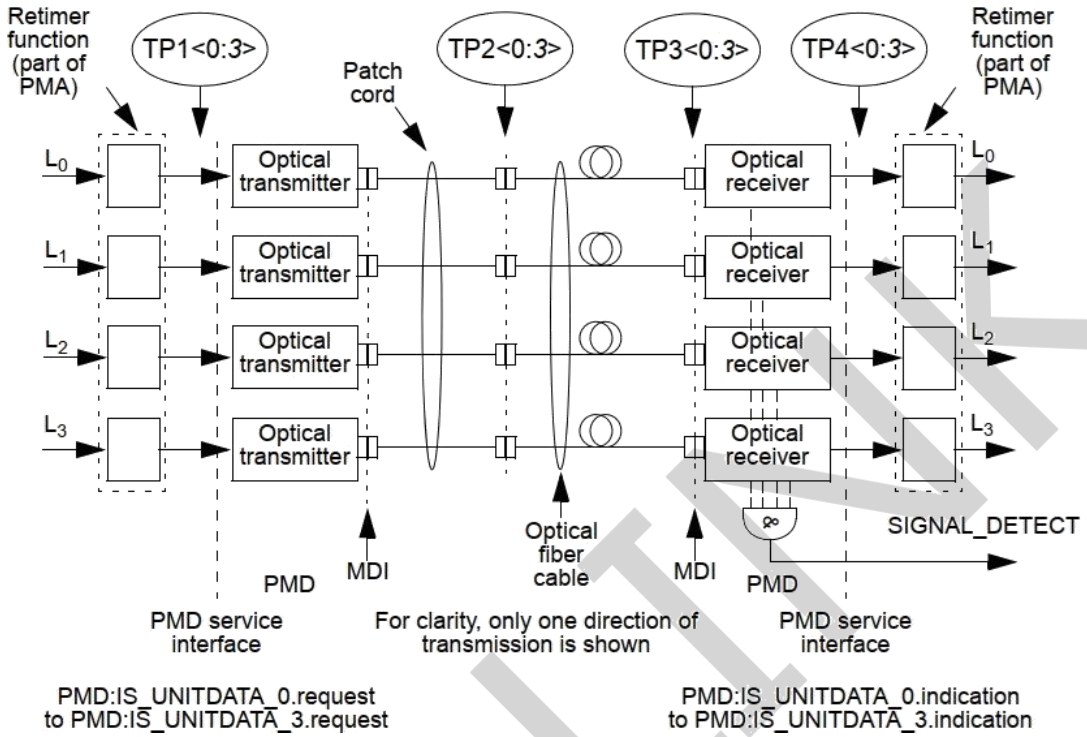


Figure 3: IEEE 802.3bm Block Diagram for 100GBASE-SR4 Transmit/Receive Paths

(The block diagram for 200GBASE-SR8 is equivalent to Figure 3, but eight lanes per direction)

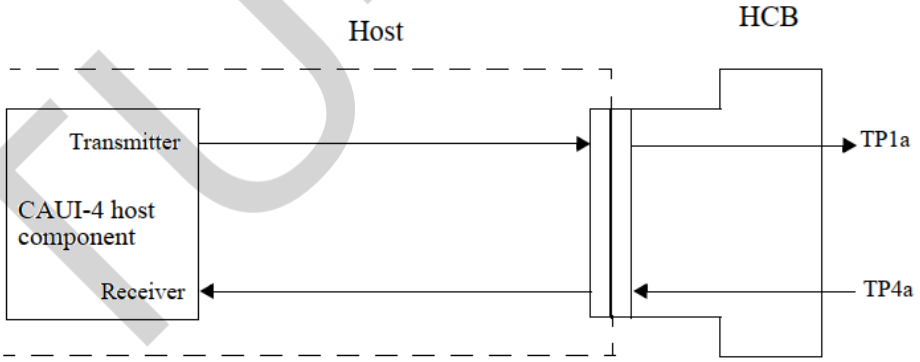


Figure 4: IEEE 802.3bm CAUI-4 C2M Compliance Points TP1a, TP4a

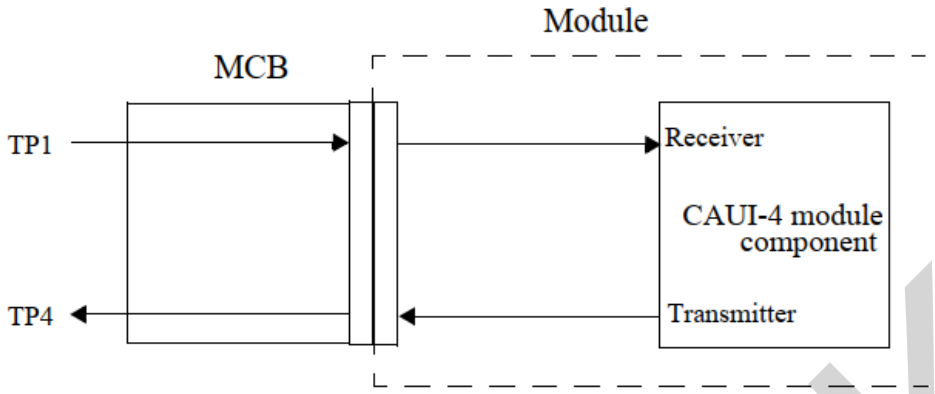


Figure 5: IEEE 802.3bm CAUI-4 C2M Compliance Points TP1, TP4

High Speed Electrical Input Characteristics

Unless otherwise stated, the following characteristics are defined under recommended operating conditions.

Parameter	Test Point	Min.	Typical	Max.	Unit
Signaling Rate, Per Lane	TP1		25.78125 ±100ppm		GBd
Differential peak-peak Input Voltage Tolerance	TP1a	900			mV
Differential Input Return Loss	TP1	Equation (83E-5) *9			dB
Common Mode to Differential Return Loss	TP1	Equation (83E-6) *9			dB
Differential Termination Mismatch	TP1			10	%
Single-ended Voltage Tolerance Range	TP1a	-0.4		3.3	V
DC Common Mode Output Voltage*7	TP1	-350		2850	mV
Module Stressed Input Test*8	TP1a				
Eye Width			0.46		UI
Applied peak-peak Sinusoidal Jitter			Table 88-13*10		
Eye Height			95		mV

Notes:

1. Equation(83E-5) and Equation(83E-6) refer to IEEE 802.3-2018.
2. DC common mode voltage generated by the host. Specification includes effects of ground offset voltage.
3. Meets BER specified in 83E.1.1 of IEEE 802.3-2018.
4. Table 88-13 refers to IEEE 802.3-2018.

High Speed Electrical Output Characteristics

Unless otherwise stated, the following characteristics are defined under recommended operating conditions.

Parameter	Test Point	Min.	Typ.	Max	Unit
Signaling Rate per Lane	TP4	25.78125± 100ppm			Gbps
AC Common-mode Output Voltage (RMS)	TP4			17.5	mV
Differential peak-to-peak Output Voltage	TP4			900	mV
Eye Width	TP4	0.57			UI
Eye Height, Differential	TP4	228			mV
Vertical Eye Closure	TP4			5.5	dB
Differential Output Return Loss	TP4	Equation (83E-2)*11			
Common to Differential Mode Conversion Return Loss	TP4	Equation (83E-3)*11			
Differential Termination Mismatch	TP4			10	%
Transition Time (20% ~80%)	TP4			12	ps
DC Common Mode Voltage*12	TP4	-350		2850	mV

Notes:

1. Equation(83E-2) and Equation(83E-3) refer to IEEE 802.3-2018.
2. DC common mode voltage generated by the host. Specification includes effects of ground offset voltage.

High Speed Optical Transmitter Characteristics

Unless otherwise stated, the following characteristics are defined under recommended operating conditions.

Optical Characteristics @TP2 Test Point

Parameter	Symbol	Min.	Typical	Max.	Unit
Signaling Rate, each Lane	DR		25.78125± 100ppm		Gbps
Modulation Format			NRZ		
Center Wavelength	λ	840		860	nm
RMS Spectral Width*13	□λrms			0.6	nm
Average Launch Power, each Lane*14	Pavg	-8.4		2.4	dBm
Outer Optical Modulation Amplitude(OMA), each Lane*15	Poma	-6.4		3	dBm
Launch Power in OMA minus TDEC	OMA-TDEC	-7.3			dBm
Transmitter and Dispersion Eye Closure (TDEC),	TDEC			4.3	dB

each Lane					
Average Launch Power of OFF Transmitter, each Lane	Poff			-30	dBm
Extinction Ratio, each Lane*16	ER	2			dB
Optical Return Loss Tolerance	ORL			12	dB
Encircled Flux*17	EF	≥86% at 19 □m ≤30% at 4.5 □m			
Transmitter Eye Mask Definition {X1, X2, X3, Y1, Y2, Y3} Hit Ratio 1.5 x 10^{-3} Hit per Sample*18		{0.3, 0.38, 0.45, 0.35, 0.41, 0.5}			

Notes:

1. RMS spectral width is the standard deviation of the spectrum.
2. Output is coupled into a 50/125μm multi-mode fiber.
3. Even if the TDEC □ 0.9 dB, the OMA (min) must exceed this value.
4. Filtered, measured with a PRBS 231-1 test pattern @25.78125Gbps.
5. If measured into type A1a.2 or type A1a.3 50 □m fiber in accordance with IEC 61280-1-4.
6. Filtered, measured with a PRBS 231-1 test pattern @25.78125Gbps.

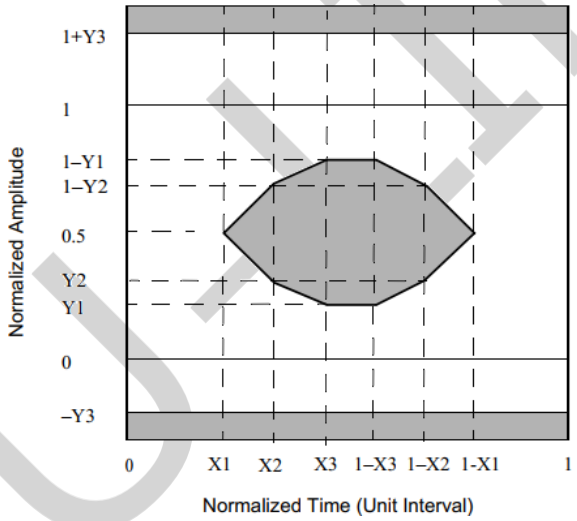


Figure 6: Transmitter eye mask definition

High Speed Optical Receiver Characteristics

Unless otherwise stated, the following characteristics are defined under recommended operating conditions.

Optical Characteristics @TP3 Test Point

Parameter	Symbol	Min.	Typical	Max.	Unit
Signaling Rate, each Lane	DR		25.78125 ±100ppm		Gbps
Modulation Format			NRZ		
Center Wavelength	λ	840		860	nm
Damage Threshold*19		3.4			dBm
Average Receiver Power, each Lane*20		-10.3		2.4	dBm
Receiver Power, each Lane (OMA)				3	dBm
Receiver Reflectance				-12	dB
Stressed Receiver Sensitivity (OMA), each Lane*21				-5.2	dBm
LOS Assert	LOSA	-20			dBm
LOS De-Assert	LOSD			-12	dBm
LOS Hysteresis	HY	0.5			dB
Conditions of Stressed Receiver Sensitivity test*22:					
Stressed Eye Closure (SEC), Lane under Test			4.3		dB
Stressed Eye J2 Jitter, Lane under Test			0.39		UI
Stressed Eye J4 Jitter, Lane under Test				0.53	UI
OMA of each Aggressor Lane			3		dBm
Stressed Receiver Eye Mask Definition {X1, X2, X3, Y1, Y2, Y3} Hit Ratio 5 x 10^{-5} Hit per Sample		{0.28, 0.5, 0.5, 0.33, 0.33, 0.4}			

Notes:

1. The receiver is able to tolerate, without damage, continuous exposure to an optical input signal having this average power level on one lane. The receiver does not have to operate correctly at this input power.
2. Average receive power, each lane (min) is informative and not the
3. principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
4. Measured with conformance test signal at TP3 for the BER less than 5E-5 with PRBS 231-1 @25.78125Gbps.
5. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

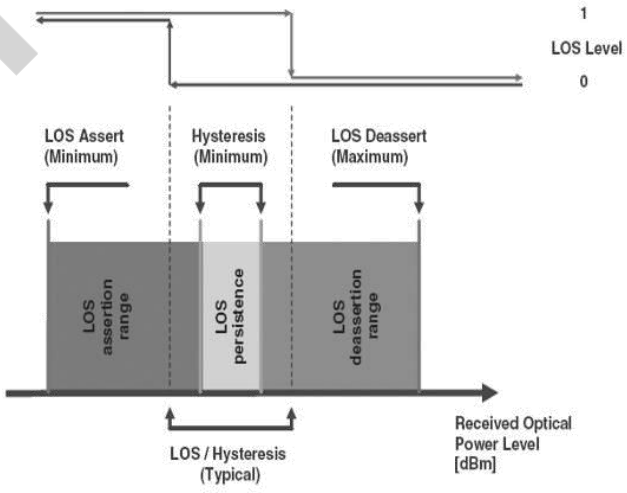
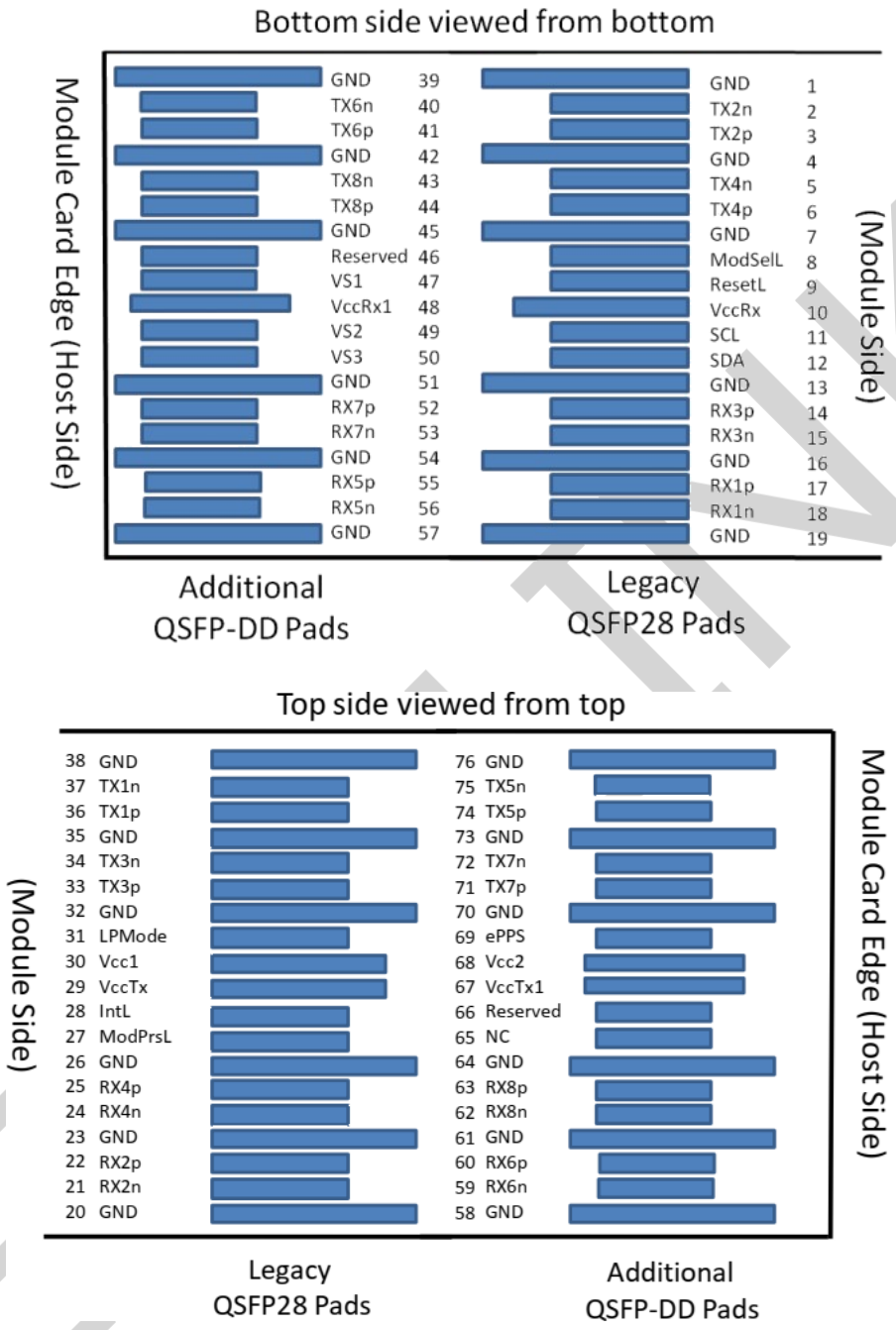


Figure 7: LOS hysteresis definition

Pin Diagram



Pin Definitions

Pin	Logic	Symbol	Description	Plug Sequence4	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1

5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		VccRx	+3.3V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3B	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL	Interrupt	3B	
29		VccTx	+3.3V Power supply transmitter	2B	2
30		Vcc1	+3.3V Power supply	2B	2
31	LVTTL-I	LPMode	Low Power Mode	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1

36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46		Reserved	For future use	3A	3
47		VS1	Module Vendor Specific 1	3A	3
48		VccRx1	3.3V Power Supply	2A	2
49		VS2	Module Vendor Specific 2	3A	3
50		VS3	Module Vendor Specific 3	3A	3
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	

63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For future use	3A	3
67		VccTx1	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2
69		Reserved	For Future Use	3A	3
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

Notes:

1. QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and
2. all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
3. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a
4. maximum current of 1000 mA.
5. All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10k ohms and less than 100 pF.
6. Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B.
7. Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B, followed by 3A, 3B.

Recommended Interface Circuit

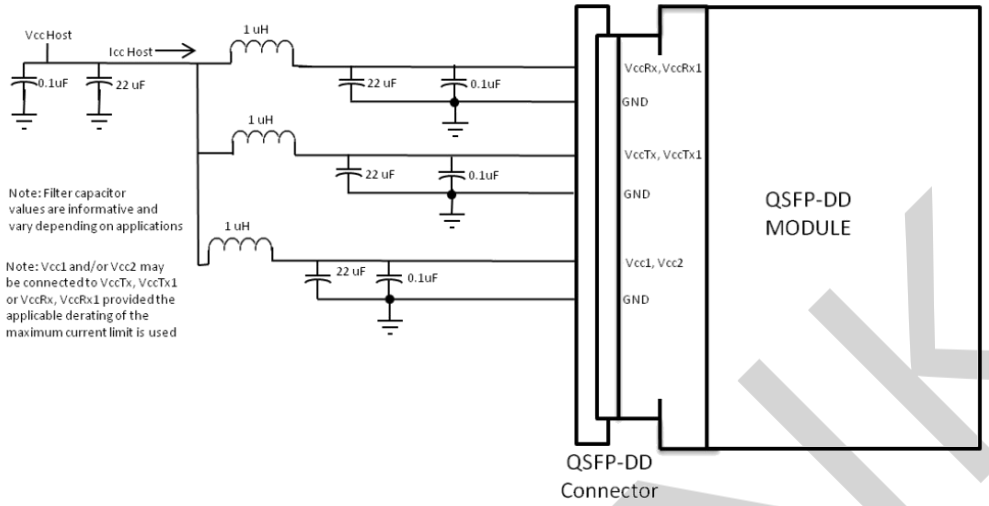


Figure 9: Host Board Power Supply Filter

Any voltage drop across a filter network on the host is counted against the host DC set point accuracy specification. Inductors with DC Resistance of less than 0.1 ohm should be used in order to maintain the required voltage at the Host Card Edge Connector. It is recommended that the 22 F capacitors each have an equivalent series resistance of 0.22 ohm.

Mechanical Diagram

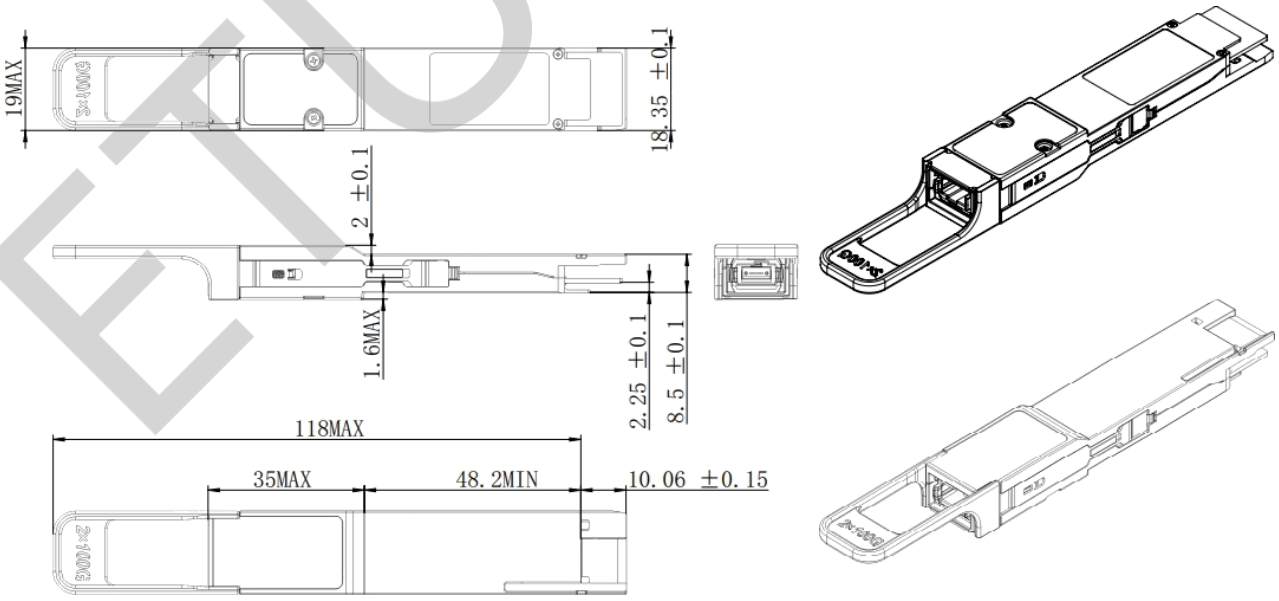


Figure 10: Mechanical Package Outline

The optical interface port is a male MPO-12 Two Row connector as specified in QSFP-DD MSA.

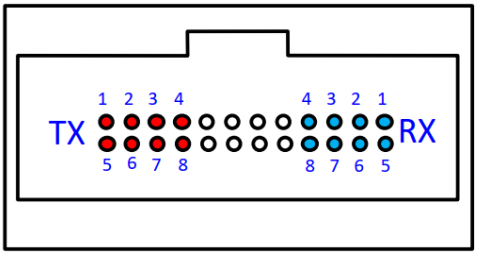


Figure 11: Module Optical Interface (looking into the optical port)

Revision History

Version No.	Date	Description
1.0	Aug 18, 2022	Preliminary datasheet
2.0	Sep 20,2024	Format change

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