EOP400-DR4

400G OSFP112 DR4 Optical Transceiver

PRODUCT FEATURES

- **OSFP form factor hot pluggable**
- **CMIS compliance**
- **4 parallel lanes of 100G-PAM4 electrical and optical parallel lanes**
- **Optical port of MPO-12/APC**
- **Up to 2km transmission**
- **9 Watts max**
- **Case temperature range of 0。C to 70。C**

APPLICATIONS

The transceiver is designed for Ethernet, Telecom and Infiniband use cases. The application advertisements listed below allow host software to select proper application following CMIS definition

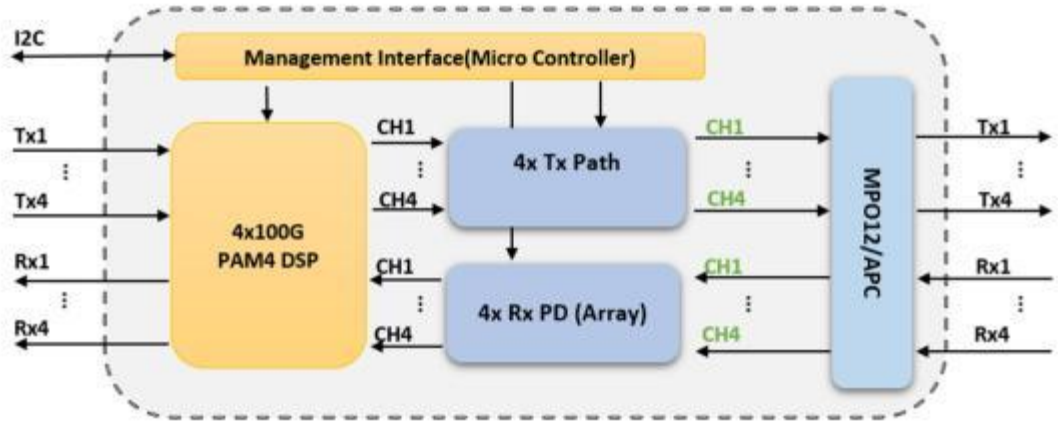
Table 1 shows CMIS application advertisements list:

ApSel Code	Host Electrical Interface	Module Media Interface	Host and Media Lane Count	Host Lane Assignment
ApSel 1	4C (100GAUI-1-L C2M)	14 (100GBASE-DR)	11 (1:1)	0F (lanes 1,2,3,4)
ApSel 2	50 (400GAUI-4-L C2M)	1C (400GBASE-DR4)	44 (4:4)	01 (lanes 1)
ApSel 3	4B (100GAUI-1-S C2M)	14 (100GBASE-DR)	11 (1:1)	0F (lanes 1,2,3,4)
ApSel 4	4F (400GAUI-4-S C2M)	1C (400GBASE-DR4)	44 (4:4)	01 (lanes 1)

DESCRIPTIONS

This product is an 400Gb/s Octal Small Form-factor Pluggable (OSFP) optical module without top open fin designed for 500m optical communication applications. The module converts 4 channels of 100Gb/s (PAM4) electrical input data to 4 channels of parallel optical signals, each capable of 100Gb/s operation for an aggregate data rate of 400Gb/s. Reversely, on the receiver side, the module converts 4 channels of parallel optical signals of 100Gb/s each channel for an aggregate data rate of 400Gb/s into 4 channels of 100Gb/s (PAM4) electrical output data.

One MPO-12 connector can be plugged into the OSFP112 DR4 module jack with 4 channels. Proper alignment is ensured by the guide pins inside the receptacle. The cable usually cannot be twisted for proper channel to channel alignment. Electrical connection is achieved through an OSFP MSA-compliant edge type connector.I2C interface is supported to read and control the status of this product. Figure 1 shows the transceiver block diagram



Ordering Information

Part No.	Data Rate(optical)	Laser	Fiber Type	Distance	Optical Interface	Temp	DDMI	Latch Color
EOP400-DR4	400Gbps	EML	SMF	500M	MPO	0~70℃	Yes	Green

Specification

It has to be noted that the operation in excess of any individual absolute maximum ratings might cause permanent damage to this module.

Parameter	Symbol	Min	Max	Units	Notes
Storage Temperature	T_S	-40	85	degC	
Operating Case Temperature	T_{OP}	0	70	degC	
Power Supply Voltage	V_{CC}	-0.5	3.6	V	
Relative Humidity (non-condensation)	RH	0	85	%	

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Units	Notes
Operating Case Temperature	T_{OP}	0		70	degC	
Power Supply Voltage	V_{CC}	3.135	3.3	3.465	V	
Data Rate, each Lane			53.125		GBd	PAM4
Data Rate Accuracy		-100		100	ppm	
Pre-FEC Bit Error Ratio				$2.4x10^{-4}$		
Post-FEC Bit Error Ratio				$1x10^{-12}$		1
Link Distance	D	0.002		2	km	2

Notes:

1. FEC provided by host system.
2. FEC required on host system to support maximum distance.

Electrical Characteristics

The following electrical characteristics are defined over the Recommended Operating Environment unless otherwise specified.

Parameter	Test Point	Min	Typical	Max	Units	Notes
Power Consumption				9	W	
Supply Current	Icc			2.72	A	
Module Input (each Lane)						
Signaling Rate, each Lane	TP1	53.125 ± 100 ppm			GBd	
DC Common-mode input Voltage	TP1	-0.35		2.85	V	
Single-ended input Voltage	TP1a	-0.4		3.3	V	
AC Common-mode RMS input Voltage Low-Frequency,VCM_{LF} Full-Band,VCM_{LF}	TP1a	 32 80			mV	
Module stressed input test		IEEE 802.3ck 120G3.4.3				
Differential Peak-to-Peak input Voltage tolerance	TP1a	750			mV	

Common to Different Mode input Return Loss	TP1	IEEE802.3ck Equation 120G-2				
Effective input Return Loss	TP1	8.5			dB	
Differential input Termination Mismatch	TP1			10	%	
Receiver (each Lane)						
Signaling Rate, each lane	TP4	53.125 ± 100 ppm			GBd	
Differential Peak-to-Peak Output Voltage Short Mode Long Mode	TP4			600 845	mV	
AC Common Mode Output Voltage, RMS Low-frequency,VCM_{LF} Full-Band,VCM_{LF}	TP4			32 80	mV	
Differential Termination Mismatch	TP4			10	%	
Vertical eye closure, VEC	TP4			12	dB	
Eye Height	TP4	15			mV	
Common-mode to Differential mode output Return Loss	TP4	IEEE802.3ck Equation 120G-1			dB	

Effective output Return Loss	TP4	8.5			dB	
Output Transition time (20% to 80%)	TP4	8.5			ps	
DC Common-mode output Voltage	TP4	-350		2850	mV	

Optical and Characteristics

Parameter	Symbol	Min	Typical	Max	Units	Notes
Wavelength	λ	1304.5	1310	1317.5	nm	
Transmitter						
Data Rate, each Lane		53.125 ± 100 ppm			GBd	

Modulation Format		PAM4				
Side-mode Suppression Ratio	SMSR	30			dB	
Average Launch Power, each Lane	P_{AVG}	-3.1		4	dBm	1
Outer Optical Modulation Amplitude (OMA_{outer}), each Lane For TDECQ ＜1.4dB For 1.4 ≤TDECQ≤3.4dB	P_{OMA}	-0.1 - 1.5+TDECQ		4.2	dBm	2
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ), each Lane	TDECQ			3.4	dB	
|TDECQ-TECQ|				2.5	dB	
Over/Undershoot				22	%	
Transmitter power excursion				2	dBm	
Extinction Ratio	ER	3.5			dB	
Transition time	Tt			17	ps	
$RIN_{17.1}OMA$	RIN			-136	dB/Hz	
Optical Return Loss Tolerance	TOL			17.1	dB	
Transmitter Reflectance	R_T			-26	dB	
Average Launch Power of OFF Transmitter, each Lane	P_{off}			-15	dBm	
Receiver						
Data Rate, each Lane		53.125 ± 100 ppm			GBd	
Modulation Format		PAM4				
Damage Threshold, each Lane	TH_d	5			dBm	3
Average Receive Power, each Lane		-7.1		4	dBm	4

Receive Power (OMA_{outer}), each Lane				4.2	dBm	
Receiver Sensitivity (OMA_{outer}),each Lane	SEN			Equation (1)	dBm	5
Stressed Receiver Sensitivity (OMA_{outer}),each Lane	SRS			-2.5	dBm	6
Receiver Reflectance	R_R			-26	dB	
LOS Assert	LOSA	-15		-9.1	dBm	
LOS De-assert	LOSD			-8.1	dBm	
LOS Hysteresis	LOSH	0.5			dB	
Conditions of Stress Receiver Sensitivity Test						
Stressed Eye Closure for PAM4 (SECQ), Lane under Test			3.4		dB	7

Notes:

1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however,a value above this does not ensure compliance.

2. The values for OMAouter (min) vary with TDECQ. Figure 5 illustrates this along with the values for OMAouter(max).

3. The receivershall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power.

4. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however,a value above this does not ensure compliance.

5. Receiver sensitivity (OMAouter) is informative and is defined for a transmitter with a value of SECQ up to 3.4 dB. Receiver sensitivity should meet Equation (1), which is illustrated in Figure 5.

RS = max (−4.5, TECQ – 5.9) dBm

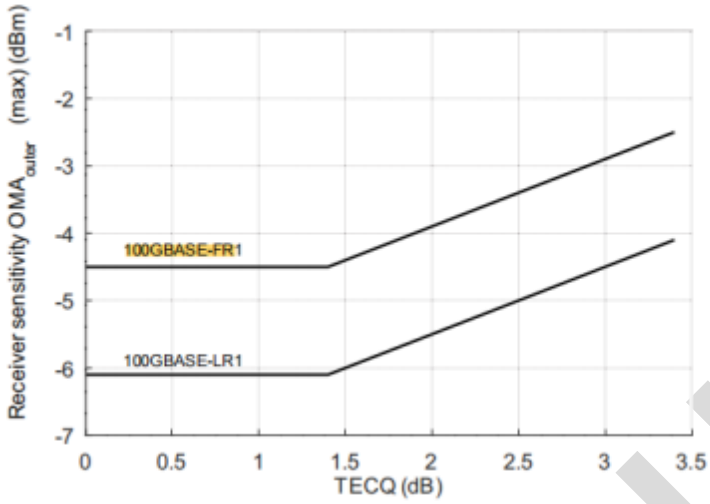
Where:

RS is the receiver sensitivity, and

TECQ is the TECQ of the transmitter used to measure the receiver sensitivity.

6. Measured with conformance test signal at TP3 for the BER equal to 2.4x10-4.

7. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.



Notes:

1.Average launch power, each lane (min) is informative and not the principal indicator of signal strength.

2. Average receive power, each lane (min) is informative and not the principal indicator of signal strength.

Digital Diagnostics

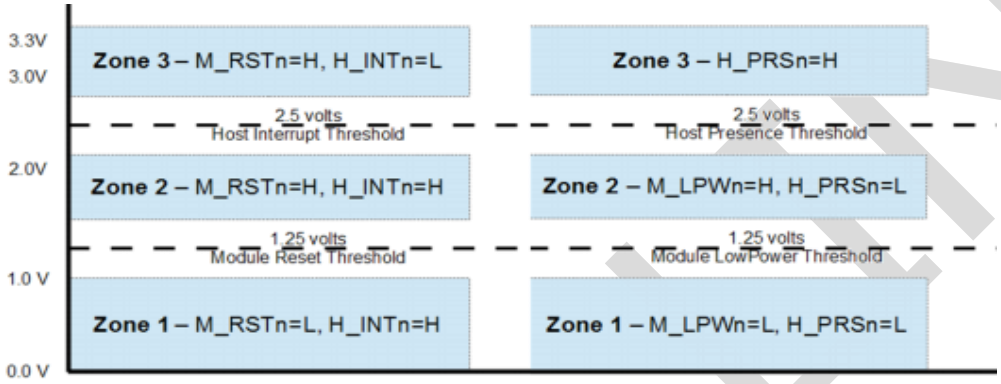
The following digital diagnostic characteristics are defined over the normal operating conditions unless otherwise specified.

Parameter	Symbol	Min	Max	Units	Notes
Temperature monitor absolute error	DMI_Temp	-3	3	degC	Over operating temperature range
Supply voltage monitor absolute error	DMI _VCC	-0.1	0.1	V	Overfull operating range
Channel RX power monitor absolute error	DMI_RX_Ch	-2	2	dB	1
Channel Bias current monitor	DMI_Ibias_Ch	-10%	10%	mA	
Channel TX power monitor absolute error	DMI_TX_Ch	-2	2	dB	1

Detailed Dontrol Pins

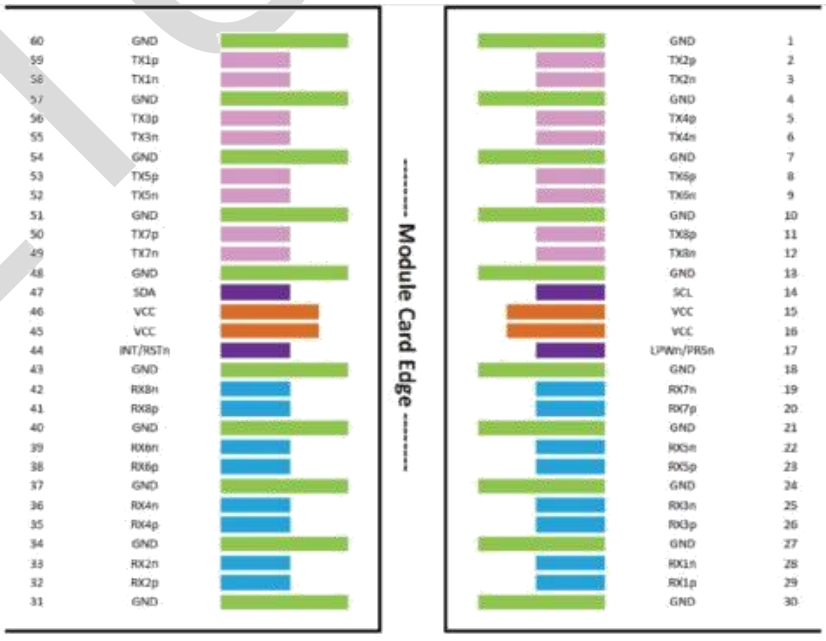
Name	Direction	Description
SCL	BiDir	2-wire serial clock signal. Requires pull-up resistor to 3.3V on host
SDA	BiDir	2-wire serial data signal. Requires pull-up resistor to 3.3V on host.

LPWn/PRSn	Input/Output	Dual Function Signal . Low Power mode is an active-low input signal . Module Present is controlled by a pull-down resistor on the module which gets converted to an active-low output logic signal Voltage zones is shown as figure3.
INT/RSTn	Input/Output	Dual Funtion Signal . Reset is an active-low input signal . Interrupt is an active-high output signal Voltage zones is shown as figure 3.



Pin Map and Description

The electrical interface of OSFP module consist of a 60 contacts edge connector as illustrated by the diagram in Figure 2, which defined in Clause 8.1 of OSFP MSA Specification.

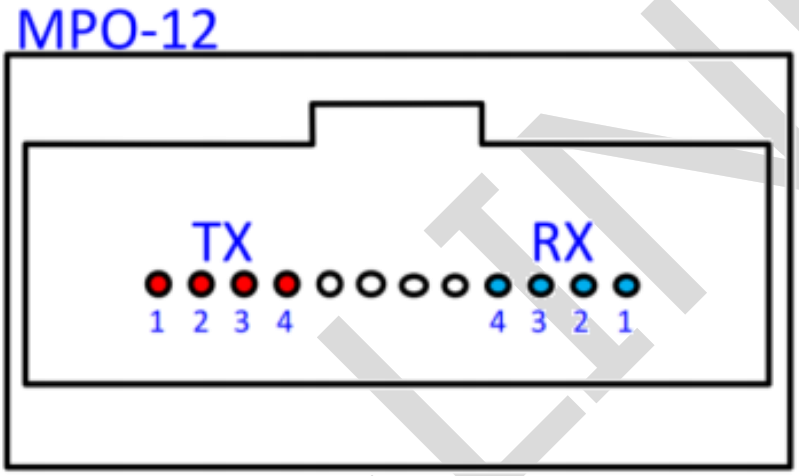


Pin#	Symbol	Description	Logic	Plug Sequence
1	GND		Ground	1
2	TX2n	Transmitter Data Inverted Input	CML-I	3
3	TX2p	Transmitter Data Non-Inverted Input	CML-I	3
4	GND		Ground	1
5	TX4n	Transmitter Data Inverted Input	CML-I	3
6	TX4p	Transmitter Data Non-Inverted Input	CML-I	3
7	GND		Ground	1
8	ModSelL	Module Select	LVTTL-I	3
9	ResetL	Module Reset	LVTTL-I	3
10	VccRx	+3.3V Power supply receiver		2
11	SCL	2-wire Serial interface clock	LVCMOS-I/O	3
12	SDA	2-wire Serial interface data	LVCMOS-I/O	3
13	GND		Ground	1
14	RX3p	Receiver Data Non-Inverted Output	CML-O	3
15	RX3n	Receiver Data Inverted Output	CML-O	3
16	GND		Ground	1
17	RX1p	Receiver Data Non-Inverted Output	CML-O	3
18	RX1n	Receiver Data Inverted Output	CML-O	3
19	GND		Ground	1
20	GND		Ground	1
21	RX2n	Receiver Data Inverted Output	CML-O	3
22	RX2p	Receiver Data Non-Inverted Output	CML-O	3
23	GND		Ground	1
24	RX4n	Receiver Data Inverted Output	CML-O	3
25	RX4p	Receiver Data Non-Inverted Output	CML-O	3
26	GND		Ground	1
27	ModPrsl	Module Present	LVTTL-O	3
28	IntL/RxLOS	Interrupt/optional RxLOS	LVTTL-O	3
29	VccTx	+3.3V Power supply transmitter		2
30	Vcc1	+3.3V Power Supply		2
31	LPMode/TxDis	Lower Power Mode/optional TX Disable	LVTTL-I	3
32	GND		Ground	1
33	TX3p	Transmitter Data Non-Inverted Input	CML-I	3
34	TX3n	Transmitter Data Inverted Input	CML-I	3

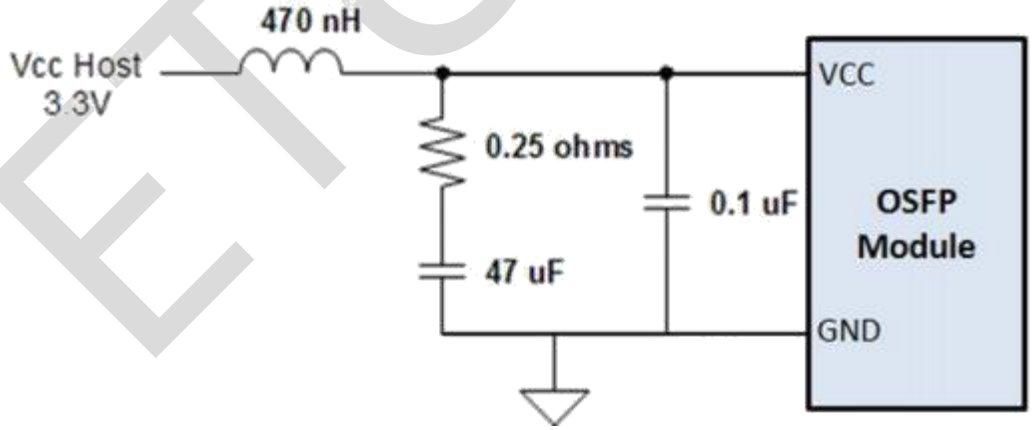
35	GND		Ground	1
36	TX1p	Transmitter Data Non-Inverted Input	CML-I	3
37	TX1n	Transmitter Data Inverted Input	CML-I	3
38	GND		Ground	1

Optical Port Description

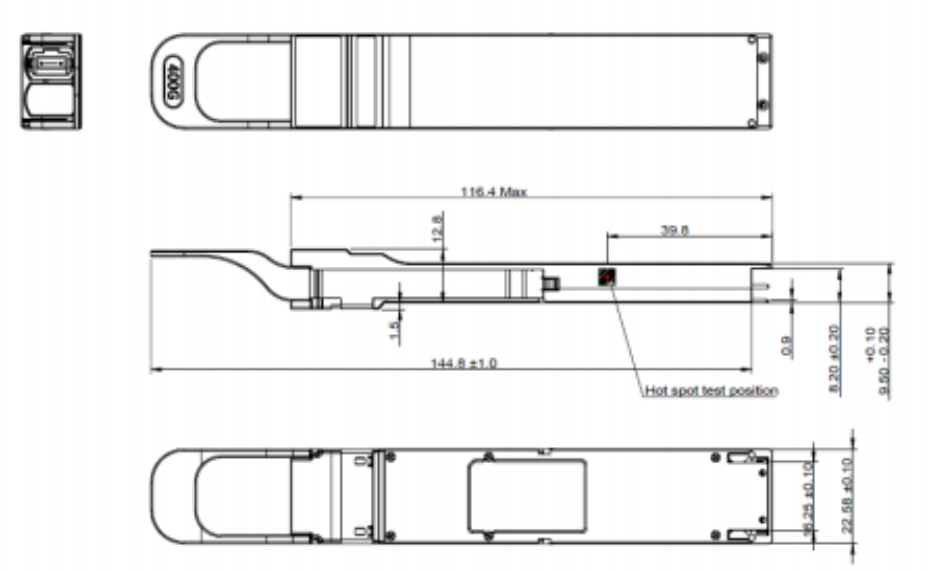
The optical interface port is an MPO-12 receptacle. The transmit and receive optical lanes shall occupy the positions depicted in Figure 4 when looking into the MDI receptacle with the connector keyway feature on top.



Recommended Interface Circuit



Mechanical Diagram



Notes:

1) the mechanical design is flattop (RHS).

2) The pull tab color is green, engraved with “400G” letter.

Revision History

Version No.	Date	Description
1.0	March 11, 2023	Preliminary datasheet
1.1	Sep 11,2024	Format change

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